Impact of ultralow phase noise oscillators on system performance

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Abstract: *While helping to understand phase noise and jitter of high-performance oscillators, this paper also examines the impact of oscillator phase noise on system performance, underscoring the importance of using ultralow phase noise oscillators in systems.*

To an electrical engineer, in an ideal world there would be no noise. But what is noise? What is electrical noise? Or more to the point of this paper: What is phase noise? As engineers, we know intuitively that low noise in a system is better than high noise. However, we must quantify this noise in commonly accepted units. We will also examine the difference in phase noise performance of commodity vs. low-cost, high-performance crystal oscillators. Understanding the cost performance trade-offs between oscillators is important to a system design. Many times we see two competitive systems separated widely in performance, but not in price. The oscillator phase noise characteristics will dominate the entire system performance and spending a few more dollars on the oscillator can boost a system's performance.

However, an engineer can easily over-specify the oscillator, and hence the key is to understand exactly how the oscillator phase noise (or jitter) limits the system performance. To help with this understanding, a tutorial on phase noise and jitter is in order.

Oscillator phase noise and jitter

In an oscillator, phase noise is the rapid random fluctuations in the phase component of the output signal. The equation of this signal is:

$$V(t) = A_0 \sin(2\pi f_0 t + \Delta\phi(t)) \qquad (1)$$

Where:

A$_0$ = nominal peak voltage
f$_0$ = nominal fundamental frequency
t = time
$\Delta\phi(t)$ = random deviation of phase from nominal — "phase noise."

Above, $\Delta\phi(t)$ is the phase noise, but A$_0$ will establish the signal-to-noise ratio. Figure 1 illustrates this.

The noise floor

Noise signals are stochastic and, in a broad sense, noise can be characterized as any undesired signal that interferes with the main signal to be processed or generated. It can disturb any physical parameter such as voltage, current, phase, frequency (or time), etc. Therefore, the idea is to maximize the signal and minimize the noise for a high signal-to-noise ratio (SNR).
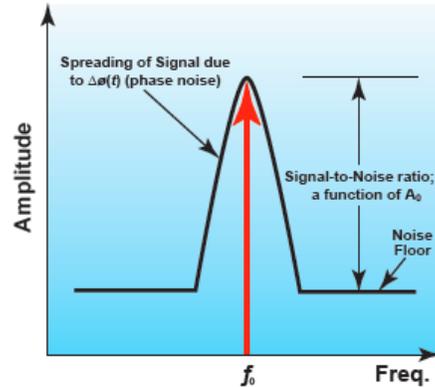
Figure 1. Frequency of domain signal (spectrum) of
$$V(t) = A_0 \sin(2\pi f_0 t + \Delta\phi(t)).$$

Noise power is quantified as
$$P_n = kT\Delta f = kTB \quad (\text{watts}) \qquad (2)$$
Where

K is the Boltzmann's constant = $1.38\text{x}10^{-23}$ (J/K)
T is the absolute temperature in K
And Δf and B both represent the *bandwidth* in which the measurement is made, in Hertz.

In the absence of any signal, there is thermal noise floor. This floor level can be specified in a variety of units: Watts, V^2/Hz, $\text{V}/\sqrt{\text{Hz}}$, dBm/Hz to name a few. For oscillators, it is convenient to use dBm/Hz to define noise density.

Before defining dBm/Hz we need to first define dBm, which refers to decibels above 1 mW in a 50 Ω system and is given by

$$dBm = 10\log(\frac{Power}{1mW}) = 10\log(\frac{V^2/R}{1mW}) \qquad (3)$$

Thus, from the above equation, 1 mW is equal to 0 dBm.

Equation 2 gives us the magnitude of thermal noise and substituting for K and T we get:

$$P_n = (1.38\text{x}10^{-23})(300)B \approx 4\text{x}10^{-21}B \text{ watts} \qquad (4)$$

Where B is the bandwidth of interest, for which we will use 1 Hz to normalize the result. Using the equation of dBm (Equation 3), and using the result from above we have:

$$P_n = 10\log\left\{(\frac{4\text{x}10^{-21}}{1\text{x}10^{-3}})B\right\} = 10\log(-17.4) + \log(B) = -174 + \log(B) \quad dBm \quad (5)$$

Setting the bandwidth B to 1 Hz will give us the final result in dBm/Hz, and since log(1) is zero, we have:

$$P_n = -174 \text{ dBm/Hz} \qquad (6)$$

The quantity of -174 dBm/Hz is the thermal noise power density of a 1 Ω resistor at 290 K measured in a 1 Hz bandwidth.

If an oscillator has an output power of 1 mW or 0 dBm, then:

$$-174 \; dBm/Hz = -174 \; dBc/Hz \qquad (7)$$

Where dBc is decibels relative to the carrier level. This result tells us that the best obtainable noise floor for a 0 dBm oscillator is -174 dBc/Hz at 290 K.

In general, one can convert dBm to dBm/Hz with:

$$dBm/Hz = (\text{value in dBm}) \text{ -10log(bandwidth)} \qquad (8)$$

and dBm/Hz to dBm with:

$$dBm = (\text{value in dBm/Hz}) \text{ +10log(bandwidth)} \qquad (9)$$

For example: What is -50 dBm in dBm/Hz in a 1 kHz bandwidth? Solution:
   Power in dBm/Hz =
   -50-10log(1000) = -50-10(3) = -80 dBm/Hz

Noise characteristics
Noise on a carrier can be separated into two categories; random and deterministic. Random noise spreads the carrier while deterministic noise generates sidebands on the carrier as illustrated in Figure 2. Adding the deterministic component to Equation 1, it now becomes,

$$V(t) = A_0 \sin[2\pi f_0 t + \Delta\phi(t) + m_d \sin(2\pi f_d t)] \qquad (10)$$

Where: m_d is the amplitude of the deterministic signal, which is phase modulating the carrier, and f_d is the frequency of the deterministic signal.

Noise has infinite bandwidth, and hence the greater the bandwidth of the instrument being used to measure a carrier frequency with noise, the higher the noise it measures. For example, as you change the resolution bandwidth (equivalent to the physical bandwidth of the IF channel) on a spectrum analyzer, the noise magnitude changes. Hence, there should be one standard measurement bandwidth to use when specifying spectral purity of an oscillator or signal source.
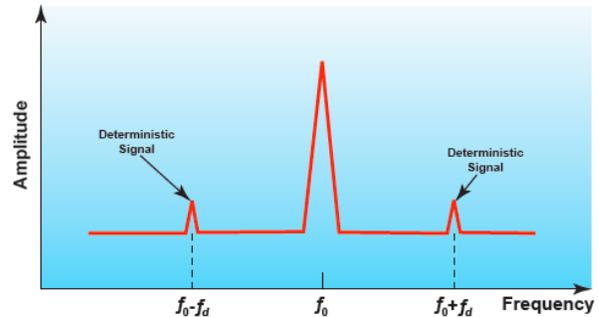
Figure 2. Frequency of
$$V(t) = A_0 \sin[2\pi f_0 t + \Delta\phi(t) + m_d \sin(2\pi f_d t)] \text{ showing}$$
deterministic signal.

The industry has settled on a correlation bandwidth for phase noise measurements of 1 Hz, known as the normalized frequency. There are few spectrum analyzers that have a 1 Hz resolution bandwidth. Such a spectrum analyzer is very expensive. In fact, the closer to the carrier you want to measure, the higher the instrument cost will be. A spectrum analyzer will specify how close to the carrier it can measure (known as the lowest resolution bandwidth possible); above this maximum frequency, one can normalize the reading to 1 Hz with the following:

$$dBc/Hz = -dBc - 10\log(\text{res. BW of spectrum analyzer}) \qquad (11)$$

For example, say the noise floor is given as -40 dBc at an offset frequency of 10 kHz from the carrier. And the resolution bandwidth of the instrument is set to 1 kHz. What is the phase noise at this point in dBc/Hz?

Answer:
$$dBc/Hz = -40 - 10\log(1000) \qquad (12)$$

Since the log(1000) = 3 we have:
$$dBc/Hz = -40 - 10(3) = -40 - (30) = -70 \qquad (13)$$

Therefore, the phase noise at this point is –70 dBc/Hz at 10 kHz offset, or:

$$L\{10\text{KHz}\} = -70\text{dBc/Hz} \qquad (14)$$

The noise spectrum of a signal is symmetrical around the carrier frequency and, therefore, it is necessary to specify only one side. This one-sided spectrum is called a single sideband (SSB) spectrum. Hence, the spectral purity of a signal can be completely quantified by its single sideband (SSB) phase noise plot as shown in Figure 3.
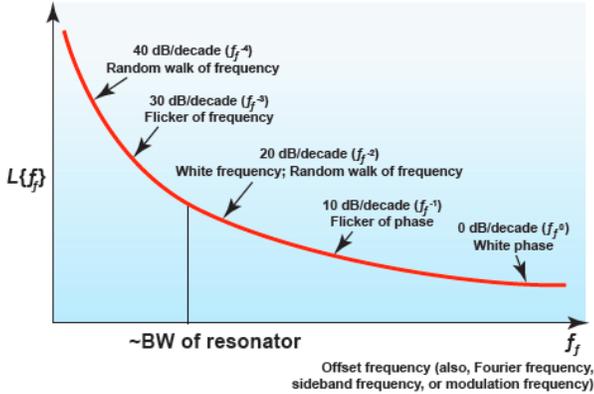
Figure 3. Typical SSB phase noise plot of oscillator vs. offset from carrier.

This SSB plot has been assigned the script L{f} and is defined as one half the sum of both sidebands. L{f} has units of decibels below the carrier per Hertz (dBc/Hz) and is defined as

$$L\{f\} = 10\log\left[\frac{P_{\text{sideband}}(f_0 + \Delta f, 1Hz)}{P_{\text{carrier}}}\right] \quad (15)$$

where $P_{\text{sideband}}(f_0 + \Delta f, 1Hz)$ represents the signal power at a frequency offset of Δf away from the carrier with a measurement bandwidth of 1 Hz.

Here are three of the most popular ways in which phase noise is defined.

1. The term most widely used to describe the characteristic randomness of frequency stability.
2. The short-term frequency instability of an oscillator in the frequency domain.
3. The peak carrier signal to the noise at a specific offset off the carrier expressed in dB below the carrier in a 1 Hz bandwidth (dBc/Hz).

Jitter and random jitter
So far, all the discussion regarding noise has been presented in the frequency domain. An oscillator noise performance characterized in the *time* domain is known as jitter. Note that phase noise and jitter are two linked quantities associated with a noisy oscillator, and, in general, as the phase noise increases in the oscillator, so does the jitter.

Jitter is a variation in the zero-crossing times of a signal, or a variation in the period of the signal. Jitter is composed of two major components, one that is predictable and one that is random. The predictable component of jitter is call *deterministic jitter*. The random component of jitter is called *random jitter*. Random jitter comes from the random phase noise, while deterministic jitter comes from the deterministic noise.

Random jitter (RJ) is characterized by a Gaussian (normal probability) distribution and assumed to be unbounded. As a result, it generally affects long-term device stability. Because peak-to-peak measurements take a long time to achieve

statistical significance, random jitter is usually measured as a root mean square (rms) value.

The Gaussian distribution is illustrated in Figure 4. Mathematically, this function is

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}}e^{-\frac{1}{2}(x-\mu)^2/\sigma^2} \quad (16)$$

Properties and notations of the Gaussian distribution are: The µ symbol designates the mean, σ designates the standard deviation and σ ² represents the variance. The Gaussian distribution is also commonly called the "normal distribution" and often referred to as a "bell-shaped curve." Note that within ±1 σ of the Gaussian distribution curve, 68.2% of the random events will occur and that 99.6% will occur within ±3 σ.
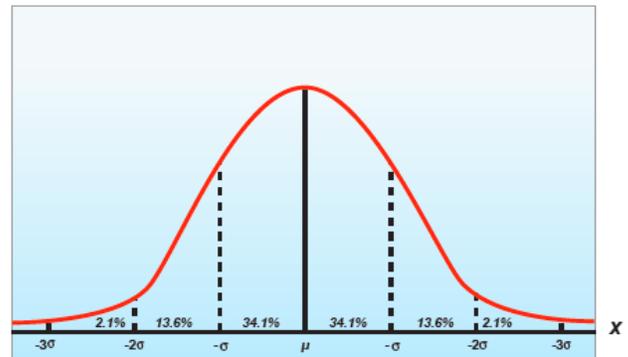
Figure 4. Gaussian or Normal distribution curve

Why does jitter take on the characteristic of a Gaussian distribution function? The answer is the following: Random jitter is the result of accumulation of random processes including thermal noise, flicker noise, shot noise, etc. All of these noise sources contribute to the total jitter observed at the output of an oscillator. The central limit theorem states that the sum of many independent random events (functions) converges to a Gaussian distribution, as depicted in Figure 5.
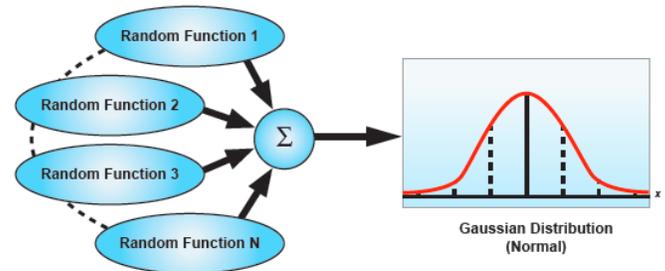
Figure 5. Central Limit Theorem – the sum of independent random functions converges to a Gaussian distribution.

Deterministic jitter (DJ)

Deterministic jitter (DJ) has a non-Gaussian probability density function (PDF) and is characterized by its bounded peak-to-peak (pk-pk) amplitude. Deterministic jitter is expressed in units of time, pk-pk. The following are examples of deterministic jitter:

- periodic jitter (PJ) or sinusoidal—e.g., caused by power supply feedthrough;
- intersymbol interference (ISI)—e.g., from channel dispersion of filtering;
- duty cycle distortion (DCD)—e.g., from asymmetric rise/fall times;
- Subharmonic(s) of the oscillator—e.g., from straight-multiplication oscillator designs;
- uncorrelated periodic jitter—e.g. from crosstalk by other signals; and

correlated periodic jitter.

Total jitter (TJ)

Total jitter (TJ) is the summation (convolution) of all independent jitter components.

Total jitter (TJ) = random jitter (RJ) + deterministic jitter (DJ)

Impact of phase noise/jitter on system

Phase noise or jitter of an oscillator has a direct impact on a system performance. In an RF communication system, high phase noise will affect communication distance, adjacent-channel interference, bit error rate (BER) to name a few.

For today's advanced high-speed converters, a clean clock signal translates to more "effective number of bits," or ENOB. The accuracy of an analog-to-digital converter (ADC) is enabled by the purity of the clock being used and its inherent SNR. Hence, a very low-jitter clock is essential to have good SNR.

In ADC converters, jitter limits the SNR by the following equation:

$$SNR = -20\log(2\pi f_{analog} t_{jitter_{rms}}) \quad in \quad dB \qquad (17)$$

Where:

f is the analog input frequency being sampled, and

t is the jitter in rms

Solving for the jitter term of the above equation, we obtain:

$$t_{jitter} = \frac{10^{-SNR/20}}{2\pi f_{analog}} \qquad (18)$$

For example, suppose we have an input signal of 80 MHz and you require an SNR of 75 dB, then a clock with 354 fs is required. This assumes that jitter is the only limiting factor in the converter performance.

Commodity clock vs. ultralow phase noise clock

We will now compare the phase difference of two oscillators, one a commodity and the other a ultralow phase noise. What dictates the title "ultralow" to some oscillator could be a matter of "specsmanship." To this author, the "ultralow phase noise" designation should be given to an oscillator with a noise floor

of –160 dBc/Hz or lower, and lower than -130 dBc/Hz at 1 kHz offset. This type of phase noise is easily achieved by many OCXO with SC-cut crystals at frequencies below 50 MHz. However, the comparison here is not for a reference type (OCXOs or TCXO for example) crystal oscillator, but rather for clock oscillators. Today, a commodity type 5 mm x 7 mm ±50 ppm stability clock can be purchased for less than $2.00. What type of phase noise are you getting from this typical commodity clock?

Crystek's oscillator family CCHD-950 (clock) and CVHD-950 (VCXO) were designed as cost-effective, clean, low jitter clocks and VCXOs. This family of oscillators uses discrete components to achieve "sub-picosecond" jitter. Figures 6 and 7 are actual SSB phase noise plots of a commodity clock and the CCHD-950 at 100 MHz. Note that when comparing jitter specs from different oscillators, it is not sufficient to simply look at the quoted jitter of 1 ps rms, max. (12 kHz to 20 MHz). Both oscillators in Figures 6 and 7 will meet this spec, but clearly the CCHD-950 is a superior oscillator in terms of phase noise and wideband jitter.
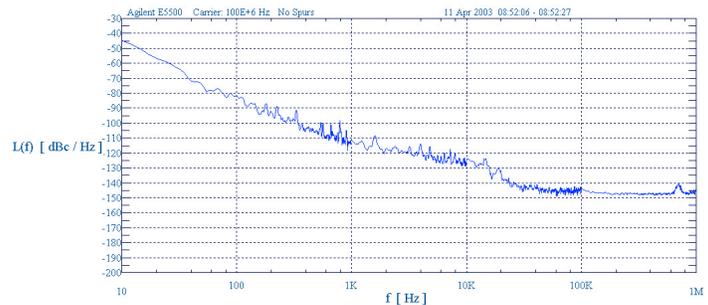
Figure 6. SSB phase noise plot of a commodity clock.
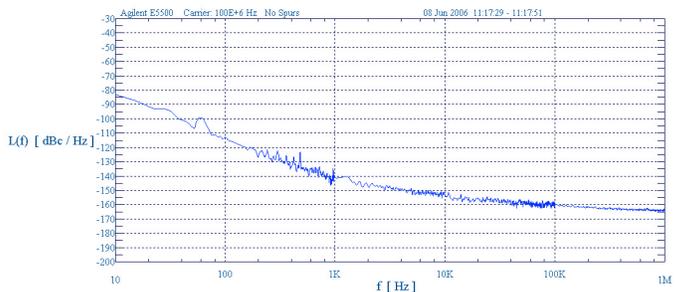
Figure 7. SSB phase noise plot of a true ultra-low phase noise oscillator (model: Crystek CCHD-950).

Achieving ultralow phase noise

A commodity oscillator is nothing more than an ASIC and a quartz crystal blank. In most cases, it does not even have an internal bypass capacitor. The crystal blank is an AT-cut strip with Q of about 25 K to 45 K. This low Q limits the close-in phase noise. The ASIC with all its transistors limits the floor noise to about -150 dBc/Hz. On the other hand, the true ultralow phase noise oscillator uses a discrete high-performance oscillator topology with a packaged crystal with a Q greater than 70 K for excellent close-in phase noise. The discrete oscillator topology establishes the SNR, and hence the floor is lower than -160 dBc/Hz. Therefore, superior performance is obtained with very high Q crystals and a good

discrete topology. This lower phase noise does come with a price delta of approximately $15. However, this a small price to pay (in most cases) considering the improvement gained.

References

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Ramón M. Cerda is Vice President of Engineering at Crystek. He holds an MSEE and BSEE from Polytechnic University of New York. Cerda has been an authority in the crystal oscillator industry for the past nine years. Prior to that, he was an RF engineer for 15 years. Cerda's specialty is high-frequency oscillator designs up to 6 GHz. These oscillator designs can be crystal, SAW, coaxial, transmission line or high Q inductor resonator based. Cerda is authoring a book on crystals and oscillators and can be reached at rcerda@crystek.com.